IN THE DRAWINGS

A proposed substitute Figure 4 is submitted herewith corrected as requested in section 5 of the Office Action.

Remarks

In view of the foregoing amendments and following remarks responsive to the Office Action of April 19, 2006, Applicant respectfully requests favorable reconsideration of this application.

Applicant respectfully thanks the Office for the indication that claim 22 is allowed, and that claims 7-14 and 19-21 are merely objected to as being dependent upon a rejected based claim.

The Office has withdrawn the previous indication of allowability of claims 1-3, 5-6, and 15-18 in view of newly discovered prior art.

Specifically, the Office rejected claims 1-3 and 15 as obvious over the admitted prior art in view of Crawford and rejected claims 5-6 and 16-18 as obvious over the admitted prior art in view of Crawford and further in view of designer's choice.

Applicant respectfully traverses. The present invention relates to an enhanced protocol for using an I2C bus. It provides enhanced addressing that increases the number of address bits so as to permit, for instance, addressing of internal registers and the like within an addressable node of the system. With reference to Figure 1 of the present application, the I2C protocol dictates that the message has a five-part format comprising: (1) a start bit 102 to initiate a transaction, (2) an address byte with 7 bits 104 denoting the address of the slave device and the eighth bit 106 denoting a read or write command, (3) 8 bit data bytes 108, (4) an acknowledgment bit 110 following each 8 bit address or data byte, and (5) a stop bit 112 to terminate the transaction. Thus, the format comprises 8 bits followed by an acknowledgment bit (transmitted in the opposite direction as the 8 bits) sandwiched between a start bit and a stop bit. The present invention is an enhanced I2C addressing scheme that permits devices to address slave devices using more than 8 bit addresses, but is still consistent with I2C protocol

requirements. Accordingly, more internal addresses within a device can be specifically addressed.

Thus, the task that must be achieved by the present invention is to accomplish greater than 8 bit addressing within the format of 8 bits followed by an acknowledgment bit, followed by 8 bits, followed by an acknowledgment bit, etc. The present invention achieves this goal by providing an 8-bit command code following the start bit 102, slave address 104, read/write bit 106, and the first acknowledgment bit 110. The command code includes a first portion (comprising two bits in the exemplary embodiments) that indicate one of three different types of addressing that will follow and, depending on the type of address that is to follow, the last six bits of the command code are the upper six bits of a 14 bit address (which would be followed, after the next acknowledgment bit 110) with 8 more bits of the 14 bit address (Figure 4 embodiment), (2) the six bits of a 6 bit supplemental address (Figure 5 embodiment), or (3) a direct command access (Figure 6 embodiment).

The Office asserted that the admitted prior art discloses all of the features of claim 1 except that a first subset of the command code bits functions as an indicator of a type of supplemental address to follow. However, the Office asserts that this is found in Crawford.

Crawford discloses a messaging protocol for communication between nodes via a bus in a motor vehicle network. The relevant portion of Crawford is found in column 6, line 64 through column 7, line 32. The messaging protocol is shown in Figure 3 of Crawford and comprises a start bit followed by a priority code, followed by a control code, followed by a function address or receiver address. It is the control code and the function address/receiver address sections of the message that the Office deems relevant. As described in column 7, lines 21 through 29, the control code indicates whether the message is a node-to-node message (in which case an address of the receiver node will appear in the function address/receiver address section of the

message) or a functional message (which is intended for global broadcast distribution to all nodes on the network, and therefore requires no address per se in the function address/receiver address portion of the message). Rather, for functional messages, the "function address" is not an address at all, but is a definition of the class of nodes to which it pertains followed by an instruction for those nodes, e.g., "headlamps" followed by "on" or "off", or "door locks" followed by "lock" or "unlock". See column 7, lines 65 through column 8, line 10.

Applicant respectfully traverses the rejection because the references are not properly combinable as there is no suggestion in the prior art to make such a combination. Particularly, as previously noted, the innovation of the present invention is the development of an efficient technique to permit multiple modes of supplemental addressing within the 8-bit-followed-by-an-acknowledgement-bit protocol of the I2C system. Crawford has no such restrictions. Crawford has simply developed a proprietary messaging protocol that has no pre-existing limitations to which it must adhere. He has started from scratch. Accordingly, the fact that Crawford may have a control code indicating a type of address that will follow teaches essentially nothing in the context of an I2C bus, which must follow a pre-ordained messaging protocol.

There would be no motivation to look to Crawford in the context of an I2C bus because Crawford's messaging protocol is entirely custom and could not fit within the I2C messaging protocol. The creative achievement of the present invention is fitting both a code that indicates the type of supplemental addressing as well as the supplemental address within the I2C format. Crawford simply does not address this issue.

Accordingly, claim 1 distinguishes over the prior art of record. Applicant has amended claim 1 to bring into the body of the claim the fact that the messaging scheme is within the I2C bus and also to improve its form in other respects.

Claim 2 even further distinguishes over the prior art of record. Particularly, the Office asserted that the admitted prior art discloses that the slave device comprises at least one internal device having an internal address and wherein said interpreting step comprises using said supplemental address to determine at least part of said internal address (specification, page 2, second paragraph). However, this is not true. Claim 2 depends from claim 1, which recites that the supplemental address is contained in the command code. However, in the admitted prior art, page 2, second paragraph, the supplemental address is in a separate byte, namely, the first data byte position. Accordingly, the admitted prior art, in fact, does not teach what is recited in claim 2.

Dependent claim 3 depends from claim 1 and, therefore, is allowable for at least all of the reasons set forth above in connection with claim 1.

Dependent claims 5 and 6, which were rejected over the admitted prior art in view of Crawford and further in view of designer's choice depend from claims 1 and 2, respectively. Accordingly, they distinguish over the prior art of record for at least all of the reasons set forth above with respect to claims 1 and 2, respectively, since the addition of "designer's choice" does not solve the shortcomings of the prior art discussed above in connection with claims 1 and 2.

With respect to claim 15, Applicant has herein amended claim 15 to incorporate the limitations of claim 19, which the Office has merely objected to. Accordingly, claim 15 and all of its dependent claims should now be in allowable form.

As previously noted, the Office has indicated that claim 22 is allowed. Applicant has herein added new apparatus claim 23, which essentially parallels the language of allowed claim 22 and, therefore, should also be allowable.

In view of the foregoing amendments and remarks, it is respectfully submitted that this application is now in condition for allowance. Applicant respectfully requests the Office to issue a Notice of Allowance at the earliest possible date. The Examiner is invited to contact Applicant's undersigned counsel by telephone call in order to further the prosecution of this case in any way.

Respectfully submitted,

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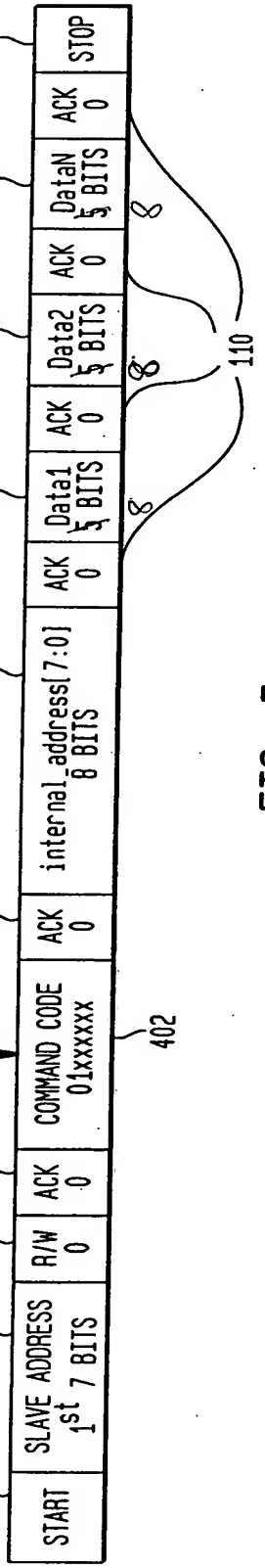

FIG. 4

WHERE XXXXXX ARE internal_address[13:8]

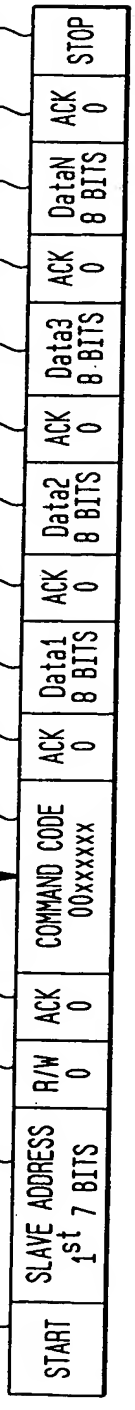

FIG. 5

WHERE XXXXXX ARE internal_address[5:0]
AND internal_address[13:8] ARE SET TO ZERO'S

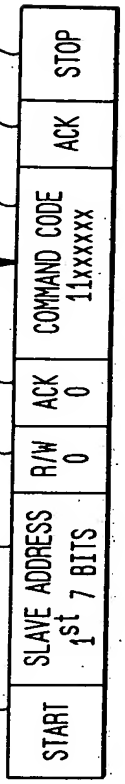

FIG. 6

WHERE XXXXXX IS THE DESIRED WRITE COMMAND TO SELECTED REGISTERS